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10/511,759	10/19/2004	Kari Pajukoski	60091.00345	4940

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EXAMINER
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NGUYEN, LEON VIET Q

ART UNIT	PAPER NUMBER
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2635

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

# Office Action Summary

Application No.

10/511,759

Applicant(s)

PAJUKOSKI, KARI

Examiner

Leon-Viet Q. Nguyen

Art Unit

2635

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 19 October 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☒ Claim(s) 21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 10/19/2004.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Information Disclosure Statement***

1. The information disclosure statement (IDS) submitted on 10/19/2004 was filed after the mailing date of 10/19/2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Claim Objections***

2. Claim 21 is objected to as failing to define the invention in the manner required by 35 U.S.C. 112, second paragraph.

The claim(s) are narrative in form and replete with indefinite and functional or operational language. The structure which goes to make up the device must be clearly and positively specified. The structure must be organized and correlated in such a manner as to present a complete operative device. The claim(s) must be in one sentence form only. Note the format of the claims in the patent(s) cited.

For the purpose of this examination, the examiner will disregard the period after "means for combining at least two filtered signals to a combination signal. "

Appropriate action is required.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1-2, 4-7, 11, 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuoka et al (US6418173).

Re claim 1, Matsuoka discloses a method for limiting a signal in a transmitter (col. 2 lines 31-34) at chip level, the method comprising:  
determining a limiting signal (115, 116) from a transmissible signal (113, col. 5 lines 5-7) filtered using a pulse shaping filter (103),  
determining an error signal (the output 119 from 107) using the transmissible signal (113) and the limiting signal (115, 116),  
generating a limited transmissible signal (122) by reducing an error signal (col. 6 lines 10-11, the distortion components includes the distortion compensation signal which is interpreted as the error signal and has a limited or reduced amplitude) filtered using the filter matched to a chip pulse waveform from the transmissible signal (107).

Re claim 2, Matsuoka discloses a method for limiting a signal in a transmitter (col. 2 lines 31-34) at chip level, the method comprising:  
determining a limiting signal (115, 116) from a transmissible signal (113, col. 5 lines 5-7) filtered using a pulse shaping filter (103),  
determining an error signal (the output 119 from 107) using the transmissible signal (113) and the limiting signal (115, 116),  
orthogonalizing the error signal (fig. 3, 108) filtered using the filter matched to a chip pulse waveform (107),  
generating a limited transmissible signal (122) by reducing the orthogonalized error signal from the transmissible signal (col. 6 lines 10-11, the distortion components includes the distortion compensation signal which is interpreted as the error signal and has a limited or reduced amplitude).

Re claim 4, Matsuoka discloses a method wherein the transmissible signal is a baseband signal (abstract, fig. 1, 113).

Re claim 5, Matsuoka discloses a method wherein the limiting signal is a baseband signal (fig. 1, 115 and 116, the I and Q signals of the limiting signal).

Re claim 6, Matsuoka discloses a method wherein the error signal is a baseband signal (fig. 1, 119, the I and Q signals of the distortion compensation signal).

Re claim 7, Matsuoka discloses a method wherein the limiting signal (115, 116) is determined by means of a threshold value set (102) for the power or amplitude values (102, col. 5 lines 5-12).

Re claim 11, Matsuoka discloses a method wherein a second clipping stage is added (105).

Re claim 35, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 1.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 3, 15, 18-20, 22-25, 29, and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) and further in view of Uta et al (US6144694).

Re claim 3, Matsuoka teaches a method for limiting a signal in a transmitter (col. 2 lines 31-34) at chip level, the method comprising:  
determining a limiting signal (115, 116) from the combination signal (113) filtered using a pulse shaping filter (103),

determining an error signal (the output 119 from 107) using the combination signal (113) and the limiting signal (115, 116),  
dividing the error signal onto different carriers in a predetermined manner (col. 5 lines 33-36),  
generating limited transmissible signals (122) by reducing each error signal part (col. 6 lines 10-11, the distortion components includes the distortion compensation signal which is interpreted as the error signal and has a limited or reduced amplitude) filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal (107).

However Matsuoka fails to teach combining at least two signals modulated on different carriers to a combination signal. Uta teaches combining n different channels into a single multiplexed channel (fig. 8, 11-1 and 11-2 combined in 18).

Therefore taking the combined teachings of Matsuoka and Uta as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the combination method of Uta into the transmitter of Matsuoka to provide a signal that is similar to white noise so that the signals of all channels have less chance of having the same value simultaneously (col. 1 lines 51-57).

Re claim 15, Matsuoka teaches a method wherein the orthogonalization of the error signal (108) is carried out according to carriers (col. 5 lines 33-36).

Re claim 18, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 1. It is implied and necessary to have a transmitter to perform the method as claimed. Furthermore, Uta teaches the means for filtering the limited transmissible signals using the pulse-shaping filter (fig. 4, 24a).

Therefore taking the combined teachings of Matsuoka and Uta as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the combination method of Uta into the transmitter of Matsuoka to limit the bandwidth of an over-sampled signal (col. 1 lines 44-45). It would be obvious to one of ordinary skill in the art that limiting the bandwidth also reduces the unwanted noise.

Re claim 19, Matsuoka teaches a transmitter limiting transmitter (col. 2 lines 31-34) a signal at chip level, the transmitter comprising:  
means for determining a first limiting signal (115, 116) from a transmissible signal (113) filtered using a pulse shaping filter (103),  
means for determining a first error signal (107) using the transmissible signal (113) and the first limiting signal (115, 116),  
means for orthogonalizing the first error signal (fig. 3, 108) filtered using the filter matched to a chip pulse waveform (107),  
means for generating a first limited transmissible signal (123) by reducing the orthogonalized first error signal from the transmissible signal (col. 6 lines 10-11, the



distortion components includes the distortion compensation signal which is interpreted as the error signal and has a limited or reduced amplitude),  
means for determining a second limiting signal (117) from the first limited transmissible signal (123) filtered using the pulse shaping filter (105 and 112, col. 5 lines 26-28),  
means for determining a second error signal (107) using the first limited transmissible signal (123) and the second limiting signal (117),  
means for generating a second limited transmissible signal (122) by reducing the second error signal (col. 6 lines 10-11, the distortion components includes the distortion compensation signal which is interpreted as the error signal and has a limited or reduced amplitude) filtered using the filter matched to a chip pulse waveform from the transmissible signal (107).

However Matsuoka fails to teach a means for filtering the second limited transmissible signal using the pulse shaping filter. Uta teaches the means for filtering the limited transmissible signals using the pulse-shaping filter (fig. 4, 24a), as previously rejected in claim 18.

Re claim 20, Matsuoka teaches a transmitter limiting a signal (col. 2 lines 31-34) at chip level, the transmitter comprising:  
means for determining a limiting signal (115, 116) from the combination signal (113) filtered using a pulse shaping filter (103),  
means for determining an error signal (the output 119 from 107) using the combination signal and the limiting signal (115, 116),

means for dividing the error signal onto different carriers in a predetermined manner (col. 5 lines 33-36),

means for generating limited transmissible signals (122) by reducing each error signal part (col. 6 lines 10-11, the distortion components includes the distortion compensation signal which is interpreted as the error signal and has a limited or reduced amplitude) filtered using the filter matched to a chip pulse waveform from a corresponding transmissible signal (107).

However Matsuoka fails to teach a means for combining at least two signals modulated on different carriers to a combination signal, means for filtering the limited transmissible signals using the pulse shaping filter, and means for generating a combined limited transmissible signal by combining the filtered limited transmissible signals. Uta teaches combining  $n$  different channels into a single multiplexed signal (fig. 8, 11-1 and 11-2 combined in 18), using a baseband filter to filter the multiplexed signal (fig. 4, 24a), and combining the split multiplexed signals (22-1, 22-2) into a single signal (the output of 44).

Therefore taking the combined teachings of Matsuoka and Uta as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the combination method of Uta into the transmitter of Matsuoka to provide a signal that is similar to white noise so that the signals of all channels have less chance of having the same value simultaneously (col. 1 lines 51-57) and to limit the bandwidth of an over-sampled signal (col. 1 lines 44-45). It would be obvious to one of ordinary skill in the art to limit the bandwidth to reduce unwanted noise.

Re claim 22, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 4.

Re claim 23, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 5.

Re claim 24, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 6.

Re claim 25, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 7.

Re claim 29, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 15.

Re claim 36, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 19.

Re claim 37, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 20.

5. Claims 8-9 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) and further in view of Piirainen et al (US20030219079A1).

Re claim 8, Matsuoka teaches a method wherein the limiting signal (115, 116) is determined by means of a threshold value set (102) for the power or amplitude values (102, col. 5 lines 5-12). However Matsuoka fails to teach the threshold value being set bearing in mind the maximum value predetermined for an error vector magnitude. Piirainen teaches considering the allowed maximum value of the error vector magnitude, or EVM, when determining a threshold value (§0031).

Therefore taking the combined teachings of Matsuoka and Piirainen as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of taking the EVM into consideration when formulating threshold values into the transmitter of Matsuoka to improve the quality of modulation (§0034).

Re claim 9, Matsuoka teaches a method wherein the limiting signal (115, 116) is determined by means of a threshold value set (102) for the power or amplitude values (102, col. 5 lines 5-12). However Matsuoka fails to teach the threshold value being set bearing in mind the maximum value predetermined for a peak code domain error. Piirainen teaches considering the maximum value of the peak code domain error used in WDMA systems when determining a threshold value (§0031).

Therefore taking the combined teachings of Matsuoka and Piirainen as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of taking the peak code domain error into consideration when formulating threshold values into the transmitter of Matsuoka to determine if there is an error in the composed signal resulting from inaccurate modulation (§0031).

Re claim 26, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 8.

Re claim 27, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 9.

6. Claims 8 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) and further in view of Smith et al (US20060146924).

Re claim 8, Matsuoka teaches a method wherein the limiting signal (115, 116) is determined by means of a threshold value set (102) for the power or amplitude values (102, col. 5 lines 5-12). However Matsuoka fails to teach the threshold value being set bearing in mind the maximum value predetermined for an error vector magnitude. Smith teaches defining a maximum error vector magnitude, or EVM, for a symbol in an

I/Q plane of a QPSK signal and determining if the EVM threshold has been breached (¶0057). Furthermore Smith teaches using a multi-tiered set of EVM masks (¶0057).

Therefore taking the combined teachings of Matsuoka and Smith as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of EVM masks as a threshold element into the transmitter of Matsuoka to determine if a signal-to-noise ratio is lower than desired and to improve the granularity of the EVM and signal-to-noise ratio estimate (¶0057).

Re claim 26, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 8.

7. Claims 10 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) and further in view of Pierzga et al (US20020114270A1).

Re claim 10, Matsuoka teaches a method wherein the limiting signal (115, 116) is determined by means of a threshold value set (102) for the power or amplitude values (102, col. 5 lines 5-12). However Matsuoka fails to teach the threshold value being set so as to obtain the desired Peak-to-Mean Ratio, Peak-to-Average Ratio, Crest factor of the power or amplitude. Pierzga teaches the use of a peak-to-mean reduction circuit (132) to detect whether any samples within a signal period are in excess of a predetermined threshold (¶0144).

Therefore taking the combined teachings of Matsuoka and Pierzga as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the reduction circuit of Pierzga into the transmitter of Matsuoka to alleviate the problem of distortion and intermodulation (§0144). Furthermore, it is well known in the art that the peak-to-mean ratio, peak-to-average ratio, and crest factor are inter-related and it would have been obvious and necessitated to use the reduction circuit to reduce the peak-to-average ratio and crest factor.

Re claim 28, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 10:

8. Claims 12 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173).

Re claim 12, it is well known in the art that the equation as claimed is merely the standard form for a system of linear equations.

Re claim 32, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 12.

9. Claims 13 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) and further in view of Currivan et al (US7110434).

Re claim 13, Matsuoka fails to teach a method wherein unused codes are utilized

in orthogonalization. However Currivan teaches using a linear combination of unused codes to cancel interference (col. 2 lines 31-33), those being orthogonal codes (col. 19 lines 56-58). It is well known in the art that orthogonal transformation is used to facilitate interference cancellation (col. 24 lines 9-14).

Therefore taking the combined teachings of Matsuoka and Currivan as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of unused codes as taught by Currivan into the transmitter of Matsuoka to cancel interference (col. 2 lines 31-33).

Re claim 33, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 13.

10. Claims 14 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) in view of Zehavi (US5602833).

Re claim 14, Matsuoka fails to teach a method wherein codes used at a lower modulation level are utilized in orthogonalization. However Zehavi teaches using lower order modulation values of  $M$  (col. 18 lines 19-26) to be used in orthogonal functions (col. 18 lines 27-31).

Therefore taking the combined teachings of Matsuoka and Zehavi as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of using lower modulation values of Zehavi into the



transmitter of Matsuoka to increase the energy of modulation symbols (col. 18 lines 15-17) and save memory space by re-using codes.

Re claim 34, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 14.

11. Claims 16-17 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173), in view of Uta et al (US6144694) and further in view of Billsberry (US20030001669).

Re claim 16, Matsuoka and Uta fail to teach a method wherein the error signal is divided equally between different carriers. However Billsberry teaches the use of an error signal splitter to divide an error signal output into equal strength portions (§0027).

Therefore taking the combined teachings of Matsuoka, Uta and Billsberry as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the error signal splitter of Billsberry into the transmitter of Matsuoka and Uta to cancel distortion in the signal at the RF output (§0027).

Re claim 17, Matsuoka and Uta fail to teach a method wherein the error signal is divided between different carriers in relation to the power or amplitude values to be

clipped. However Billsberry teaches an error splitter that apportions an error signal according to the magnitudes of the signals input into the splitter (§0027).

Therefore taking the combined teachings of Matsuoka, Uta and Billsberry as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the error signal splitter of Billsberry into the transmitter of Matsuoka and Uta to cancel distortion in the signal at the RF output (§0027).

Re claim 30, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 16.

Re claim 31, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 17.

12. Claims 21 and 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuoka et al (US6418173) in view of Uta et al (US6144694) and further in view of Hiramatsu et al (EP0993136A1).

Re claim 21, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 20. However Matsuoka and Uta fail to teach a means for filtering transmissible signals modulated on different carriers using

pulse shaping filters. Hiramatsu does teach using band pass filtering on different transmission signals (fig. 2, 124 to 127).

Therefore taking the combined teachings of Matsuoka, Uta, and Hiramatsu as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the filtering of Hiramatsu into the method of Uta and the transmitter of Matsuoka to reduce calculation scale or circuit scale in a peak power calculation circuit (¶0017).

Re claim 38, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 21.

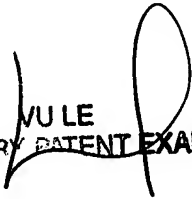
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on 571-272-7332. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Nguyen/

  
**SUPERVISORY PATENT EXAMINER**